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FISH & RICHARDSON P.C. (BO)
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
GAMI, TEJAL	

ART UNIT	PAPER NUMBER
2121	

NOTIFICATION DATE	DELIVERY MODE
02/08/2011	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATDOCTC@fr.com

Office Action Summary	Application No.	Applicant(s)	
	10/528,956	OBERHOFFNER ET AL.	
	Examiner	Art Unit	
	TEJAL J. GAMI	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *28 May 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *04/09/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to a REQUEST FOR CONTINUED EXAMINATION entered May 28, 2010 for the patent application 10/528956.

Status of Claims

2. Claims 1-20 were rejected in the last Office Action dated November 9, 2009.

As a response to the November 9, 2009 office action, Applicant has Amended claims 1, 2, 8-10, 12, 16, and 17.

Claims 1-20 are now presented for examination in this office action.

Claim Objections

3. Examiner thanks applicant for amending the claims in response to the objections presented in the previous office action. Those objections have been withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Hyatt (U.S. Patent Number: 5,339,275).

As to independent claim 1, Hyatt discloses a controller (e.g., memory controller) (see Col. 4, Line 4) comprising:

a control circuit (e.g., Figure 9F) comprising a closed loop circuit (e.g., circuit 996; output signal 965 is fedback in servo form to multiplier 980 to close a servo loop) (see Col. 63, Lines 42-44; and Figure 9I), the closed loop circuit comprising:

an input (e.g., signal 936; and decoder signals 990) (see Figure 9I and Figure 9F);

an output (e.g., output signal 965; and signal 960) (see Col. 63, Lines 42-44; Figure 9I and Figure 9F);

a forward path coupled to the input and to the output (e.g., recirculation path 960; output signal 965 is fedback in servo form to multiplier 980 to close a servo loop) (see Col. 63, Lines 42-44; and Figure 9I and Figure 9F);

a feedback path coupled to the input and to the output (e.g., recirculation path 960; output signal 965 is fedback in servo form to multiplier 980 to close a servo loop) (see Col. 63, Lines 42-44; and Figure 9I and Figure 9F); and

a sensor having a sensitivity (e.g., refresh circuitry may sample the reference signal as indicative of the magnitude of the degradation and may refresh the analog signals from the analog memory in response to the amount of degradation of the reference signal) (see Col. 50, Lines 42-63), the sensor (e.g., refresh circuit 996) being in the forward path or in the feedback path (see Figure 9F), the sensor (e.g., refresh circuit 996) (see Figure 9F) for generating a sensor

signal (e.g., to generated refreshed or compensated output signal 960) (see Figure 9F and 9H; and Col. 65, Lines 17-21);

an error signal generator that is external to the closed loop circuit (e.g., CCD error mechanism) the error signal generator to generate an error signal (e.g., bias errors) (see Col. 64, Line 63 to Col. 65, Line 4) and to provide the error signal to the closed loop circuit such that the error signal is incorporated into a useful signal of the closed loop circuit (e.g., bias reference signal will be shifted out of CCD memory 932 to refresh circuit 996 for compensating the data signal 936 for bias errors) (see Figure 9F; and Col. 65, Lines 14-17), wherein the error signal is predetermined (e.g., bias errors) (see Col. 65, Lines 2-4), the closed loop circuit being configured to generate an output signal at an output of the closed loop circuit (e.g., out of CCD memory 932 to refresh circuit 996) (see Figure 9F; and Col. 65, Lines 14-17), the output signal being based on the sensor signal and the error signal (e.g., data signal 936 for bias errors) (see Figure 9F; and Col. 65, Lines 14-17), the output signal being sent along the feedback path to the input of the control circuit (e.g., to generated refreshed or compensated output signal 960) (see Figure 9F and 9H; and Col. 65, Lines 17-21); and

a detector configured to detect a change in the sensitivity of the sensor (e.g., detected degradation) (see Col. 50, Lines 42-63), the detector being coupled to the forward path (e.g., Figure 9F), the detector to generate a control signal (e.g., decoder 995 may enable loading of a new reference signal into memory 932 and may also enable sampling of the corresponding degrading reference signal as signal 936 output from memory 932 with refresh circuitry 996) (see Col. 70, Lines 45-49);

wherein the forward path comprises a control device (e.g., sample-and-hold circuit may be used to control a refresh circuit for controlling gain of an amplifier to selectively amplify the degraded analog signals to compensate for degradation caused by shifting through the analog memory) (see Col. 50, Lines 66 to Col. 51, Line 3; and Figure 9I), which is coupled to the output (e.g., analog output signal 936 is shown having an amplitude 957) (see Col. 57, Lines 57-61; and Figure 9D), to limit an output signal at the output to a predetermined value (e.g., upper limit 955 and lower limit 956) (see Col. 57, Lines 57-61; and Figure 9D), the detector to control the control device using the control signal (e.g., refresh circuitry 996 operating under control of a degraded reference signal may be used to control refresh operations as a function of actual degradation of the signal and may therefore be used over a range of degradation variables) (see Col. 61, Lines 16-20; and Col. 70, Lines 14-18).

As to independent claim 8, Hyatt discloses a method of operating a controller (e.g., memory controller) (see Col. 4, Line 4) comprised of:

a control circuit (e.g., Figure 9F) comprising a closed loop circuit (e.g., circuit 996; output signal 965 is fedback in servo form to multiplier 980 to close a servo loop) (see Col. 63, Lines 42-44; and Figure 9I), the closed loop circuit comprising:

an input (e.g., signal 936; and decoder signals 990) (see Figure 9I and Figure 9F);

an output (e.g., output signal 965; and signal 960) (see Col. 63, Lines 42-44; Figure 9I and Figure 9F);

a forward path coupled to the input and to the output (e.g., recirculation path 960; output signal 965 is fedback in servo form to multiplier 980 to close a servo loop) (see Col. 63, Lines 42-44; and Figure 9I and Figure 9F);

a feedback path coupled to the input and to the output (e.g., recirculation path 960; output signal 965 is fedback in servo form to multiplier 980 to close a servo loop) (see Col. 63, Lines 42-44; and Figure 9I and Figure 9F); and

a sensor having a sensitivity (e.g., refresh circuitry may sample the reference signal as indicative of the magnitude of the degradation and may refresh the analog signals from the analog memory in response to the amount of degradation of the reference signal) (see Col. 50, Lines 42-63), the sensor (e.g., refresh circuit 996) being in the forward path or in the feedback path (see Figure 12B), the sensor (e.g., refresh circuit 996) (see Figure 9F) generating a sensor signal (e.g., to generated refreshed or compensated output signal 960) (see Figure 9F and 9H; and Col. 65, Lines 17-21), the forward path generating an output signal based on the sensor signal (e.g., to generated refreshed or compensated output signal 960) (see Figure 9F and 9H; and Col. 65, Lines 17-21), the output signal being applied to the input of the forward path via the feedback path (see Figure 9F);

wherein the method comprises:

generating an error signal that is predetermined (e.g., CCD error mechanism), the error signal being generated outside the closed loop circuit (e.g., bias errors) (see Col. 64, Line 63 to Col. 65, Line 4);

incorporating the error signal into a useful signal of the closed loop circuit (e.g., bias reference signal will be shifted out of CCD memory 932 to refresh circuit 996 for compensating the data signal 936 for bias errors) (see Figure 9F; and Col. 65, Lines 14-17);

obtaining a measurement signal from the closed loop circuit (e.g., decoder 995 may enable loading of a new reference signal into memory 932 and may also enable sampling of the corresponding degrading reference signal as signal 936 output from memory 932 with refresh circuitry 996) (see Col. 70, Lines 45-49), the measurement signal being obtained using a detector that is coupled to the closed loop circuit (e.g., detected degradation) (see Col. 50, Lines 42-63; and Figure 9F);

generating a control signal that is indicative of a change in sensitivity of the sensor (e.g., refresh circuitry may sample the reference signal as indicative of the magnitude of the degradation and may refresh the analog signals from the analog memory in response to the amount of degradation of the reference signal) (see Col. 50, Lines 42-63), the control signal being based on comparison of the measurement signal and a stored signal (e.g., upper limit 955 and lower limit 956) (see Col. 57, Lines 57-61; and Figure 9D); and

applying the control signal to a control device in the closed loop circuit (e.g., sample-and-hold circuit may be used to control a refresh circuit for controlling gain of an amplifier to selectively amplify the degraded analog signals to compensate for degradation caused by shifting through the analog memory)

(see Col. 50, Lines 66 to Col. 51, Line 3; and Figure 9I), the control device being coupled to the output (e.g., CCD memory..discharge) (see Col. 99, Lines 36-43; and Figure 12B), and the control device limiting an output signal at the output (e.g., analog output signal 936 is shown having an amplitude 957) (see Col. 57, Lines 57-61; and Figure 9D) to a predetermined value in response to the control signal (e.g., upper limit 955 and lower limit 956) (see Col. 57, Lines 57-61; and Figure 9D).

As to independent claim 16, Hyatt discloses a controller (e.g., memory controller) (see Col. 4, Line 4) comprising:

a closed loop circuit (e.g., circuit 996; output signal 965 is fedback in servo form to multiplier 980 to close a servo loop) (see Col. 63, Lines 42-44; and Figure 9F and Figure 9I) comprising:

an input (e.g., signal 936; and decoder signals 990) (see Figure 9I and Figure 9F);

an output (e.g., output signal 965; and signal 960) (see Col. 63, Lines 42-44; Figure 9I and Figure 9F);

a forward path coupled to the input and to the output (e.g., recirculation path 960; output signal 965 is fedback in servo form to multiplier 980 to close a servo loop) (see Col. 63, Lines 42-44; and Figure 9I and Figure 9F);

a feedback path coupled to the input and to the output (e.g., recirculation path 960; output signal 965 is fedback in servo form to multiplier 980 to close a servo loop) (see Col. 63, Lines 42-44; and Figure 9I and Figure 9F); and

a sensor having a sensitivity (e.g., refresh circuitry may sample the reference signal as indicative of the magnitude of the degradation and may refresh the analog signals from the analog memory in response to the amount of degradation of the reference signal) (see Col. 50, Lines 42-63), the sensor (e.g., refresh circuit 996) being in the forward path or in the feedback path (see Figure 9F), the sensor (e.g., refresh circuit 996) (see Figure 9F) for generating a sensor signal (e.g., to generated refreshed or compensated output signal 960) (see Figure 9F and 9H; and Col. 65, Lines 17-21), the sensor signal being converted into a feedback signal (e.g., to generated refreshed or compensated output signal 960) (see Figure 9F and 9H; and Col. 65, Lines 17-21) and being applied to the input via the feedback path (see Figure 9F);

an error signal generator (e.g., CCD error mechanism) to generate an error signal (e.g., bias errors) (see Col. 64, Line 63 to Col. 65, Line 4) and to provide the error signal to the closed loop circuit such that the error signal is incorporated into a useful signal of the closed loop circuit (e.g., bias reference signal will be shifted out of CCD memory 932 to refresh circuit 996 for compensating the data signal 936 for bias errors) (see Figure 9F; and Col. 65, Lines 14-17), wherein the error signal is predetermined (e.g., bias errors) (see Col. 65, Lines 2-4) and wherein the error signal (e.g., data signal 936 for bias errors) (see Figure 9F; and Col. 65, Lines 14-17) generator (e.g., to generated refreshed or compensated output signal 960) (see Figure 9F and 9H; and Col. 65, Lines 17-21) is external to the control circuit (e.g., out of CCD memory 932 to refresh circuit 996) (see Figure 9F; and Col. 65, Lines 14-17);

a detector (e.g., detected degradation) (see Col. 50, Lines 42-63), which is coupled to the closed loop circuit (e.g., Figure 9F), the detector being configured to detect a change in sensitivity of the sensor, the detector to generate a control signal based on the change in sensitivity of the sensor (e.g., decoder 995 may enable loading of a new reference signal into memory 932 and may also enable sampling of the corresponding degrading reference signal as signal 936 output from memory 932 with refresh circuitry 996) (see Col. 70, Lines 45-49);

wherein the closed loop control circuit further comprises a control device (e.g., sample-and-hold circuit may be used to control a refresh circuit for controlling gain of an amplifier to selectively amplify the degraded analog signals to compensate for degradation caused by shifting through the analog memory) (see Col. 50, Lines 66 to Col. 51, Line 3; and Figure 9I), the control device being coupled to the output (e.g., analog output signal 936 is shown having an amplitude 957) (see Col. 57, Lines 57-61; and Figure 9D), to limit an output signal at the output to a predetermined value (e.g., upper limit 955 and lower limit 956) (see Col. 57, Lines 57-61; and Figure 9D), the control device being controlled by the control signal (e.g., refresh circuitry 996 operating under control of a degraded reference signal may be used to control refresh operations as a function of actual degradation of the signal and may therefore be used over a range of degradation variables) (see Col. 61, Lines 16-20; and Col. 70, Lines 14-18).

As to dependent claim 2, Hyatt teaches the controller of claim 1, wherein the detector (e.g., detected degradation) (see Col. 50, Lines 42-63) comprises:

a storage device (e.g., memory) to store a measurement signal (see Col. 76, Lines 36-41); and

a comparator (e.g., comparitor 617) to compare an intermediate signal to the measurement signal and to output a comparator signal, the intermediate signal being stored in the storage device (see Col. 23, Lines 36-37).

As to dependent claim 3, Hyatt teaches the controller of claim 2, wherein the detector (e.g., detected degradation) (see Col. 50, Lines 42-63) further comprises:

decision logic (e.g., comparison logic) to receive the comparator (e.g., comparator 617) signal and to control the control device in accordance with the comparator signal (see Col. 88, Lines 48-68).

As to dependent claim 4, Hyatt teaches the controller of claim 1, wherein the control device comprises a clamp circuit (see Col. 82, Lines 35-44).

As to dependent claim 5, Hyatt teaches the controller of claim 2, wherein the comparator comprises at least one of a signal level comparator and a signal sign comparator (see Col. 23, Lines 36-64).

As to dependent claim 6, Hyatt teaches the controller of claim 1, further comprising:

a time signal generator to generate a time signal output, wherein the error signal generator is configured to generate the error signal based on the time signal output (see Col. 87, Lines 56-62).

As to dependent claim 7, Hyatt teaches the controller of claim 1, wherein the sensor comprises a magnetoresistive sensor (see Col. 116, Lines 56-61).

As to dependent claim 9, Hyatt teaches the method of claim 8, wherein the measurement signal is stored in a storage device, and the comparison is performed using a comparator (see Col. 46, Lines 4-7).

As to dependent claim 10, Hyatt teaches the method of claim 8, wherein the control signal is generated via decision logic (e.g., comparison logic), the decision logic being controlled by an output signal from the comparator (see Col. 88, Lines 48-68), the decision logic generating the control signal if a predetermined criterion is satisfied (see Col. 99, Lines 36-43).

As to dependent claim 11, Hyatt teaches the method of claim 9, wherein the comparator comprises at least one of a signal sign comparator and a signal level comparator (see Col. 23, Lines 36-64).

As to dependent claim 12, Hyatt teaches the method of claim 10, wherein the error signal is generated based on an output of a time signal generator and an output of the decision logic (e.g., bias reference signal will be shifted out of CCD memory 932 to refresh circuit 996 for compensating the data signal 936 for bias errors) (see Figure 9F; and Col. 65, Lines 14-17); and

wherein the measurement signal is based on both the sensor signal and the error signal (see Col. 19, Lines 35-43).

As to dependent claim 13, Hyatt teaches the method of claim 1, wherein the control signal comprise a signal output of the detector (e.g., detected degradation) (see Col. 50, Lines 42-63).

As to dependent claim 14, Hyatt teaches the controller of claim 1, wherein the sensor generates the sensor signal based on one or more input signals applied to the input of the forward path (e.g., to generated refreshed or compensated output signal 960) (see Figure 9F and 9H; and Col. 65, Lines 17-21).

As to dependent claim 15, Hyatt teaches the method of claim 8, wherein the sensor generates the sensor signal based on one or more input signals applied to the input of the forward path (e.g., to generated refreshed or compensated output signal 960) (see Figure 9F and 9H; and Col. 65, Lines 17-21).

As to dependent claim 17, Hyatt teaches the controller of claim 16, wherein the detector (e.g., detectors 643 and 645) (see Col. 82, Lines 34-44) comprises:

a storage device (e.g., memory) to store a measurement signal (see Col. 76, Lines 36-41); and

a comparator (e.g., comparitor 617) to compare a stored signal to the measurement signal and to output a comparator signal (see Col. 23, Lines 36-37).

As to dependent claim 18, Hyatt teaches the controller of claim 17, wherein the detector (e.g., detectors 643 and 645) (see Col. 82, Lines 34-44) further comprises:

decision logic (e.g., comparison logic) to receive the comparator (e.g., comparator 617) signal and to control the control device in accordance with the comparator signal (see Col. 88, Lines 48-68).

As to dependent claim 19, Hyatt teaches the controller of claim 16, wherein the control device comprises a clamp circuit (see Col. 82, Lines 35-44).

As to dependent claim 20, Hyatt teaches the controller of claim 17, wherein the comparator comprises at least one of a signal level comparator and a signal sign comparator (see Col. 23, Lines 36-64).

Response to Arguments

6. Applicant's amendment and arguments filed May 28, 2010 have been fully considered. The amendment does not overcome the original art rejection and the arguments are not persuasive. The following are the Examiner's observations in regard thereto.

Examiner Responds:

Examiner is not persuaded. More specific examples of prior art anticipation of claim limitations are presented above. See office action above for claimed limitations anticipated by the prior art.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tejal J. Gami whose telephone number is (571) 270-1035. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ALBERT DECADY/
Supervisory Patent Examiner, Art Unit 2121

/TJG/